Low Offset Voltage and High Slew Rate Buffer Amplifier for TFT-LCD Applications

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Abstract

A high slew rate and low offset voltage buffer amplifier for TFT-LCD source driver is proposed. By employing the CMFB circuit, the offset voltage can be controlled within 1.88 mV. Besides, by integrating the slew rate enhancing circuit, the settling time can be effectively reduced. The proposed buffer features a large output swing of 4.6 V and low power consumption of 1.98 mV with a 5 V power supply. This buffer is suitable for large-size TFT- LCDs and LCD-TVs applications.

1. Introduction

For LCD-TV and multimedia applications, TFT-LCD panels become larger and usually have heavy loads in scan/data lines on array. In generally, large-size LCD-TVs require high color depth and high resolution to show full color and high definition images. Hence, a large driving capability and low offset voltage buffer in source driver ICs is necessary.

In the operational amplifier, the sources of the offset are aware of the systematic offset and the random offset. According to the input and output common-mode voltage, the systematic offset arises due to channel length modulation of transistors and the magnitudes of the offset voltage are different. The random offset arises by the variations of the physical parameters of transistors after fabrication. [1]

In CMOS technology, the output buffer for TFT-LCD driving application has been studied. [2-5] In the input differential pair, because the device aging and mismatch resulting from the fabrication processes cause the variations of the parameters on the CMOS devices, the circuit of output buffer easily suffers from an offset voltage. Thus, the brightness of the pixels will be different and result in "mura" because the pixel voltages for the same gray levels are driven through the buffers with large offset voltages.

For a high resolution LCD-TVs, due to the data lines with heavy RC loads, the charging/ discharging time of the pixel capacitance becomes shorter and thus the pixel voltage needs a more accuracy value. In prior literatures, many methods have been proposed to reduce the affection of the offset voltage and speed up the slew rate of the buffers in source driver ICs. [2-5] Lim et al. [2] and Chan et al. [3] reach the offset voltage less than 1 mV, but the circuits had sets of extra current sources and not large enough output swing. The circuit in ref. [4] can accelerate the rising and falling times, but it only decreases either rising or falling time.

In this work, the common-mode feedback (CMFB) circuit and the slew rate enhancing skill were used. The CMFB circuit provides an additional feedback loop and defines the common-mode voltages which can reduce the offset voltage of the buffer. Two comparators and auxiliary transistors can reach high speed charging/discharging for output loads. So, the proposed buffer is suitable for high color depth and high-resolution LCD-TV applications.

2. Proposed Circuit

Figure 1 shows the block diagram of the proposed high slew rate and low offset voltage buffer. This circuit includes three main parts: the fully-differential input stage (M4-M8), the CMFB stage (M13-M15), and the slew rate enhancing output stage (M16-M17). Generally, the fully-differential output voltages have two components, the differential-mode and common- mode signals. Now, they are used to the input of the CMFB stage that can reduce the affection of the differential-mode signal. Two comparators, Com_p and Com_n, and the auxiliary transistors, M18 and M19, are used to enhance the slew rate (SR) of the output voltage. In the stable stage, if the output voltage of Com_p is "H", the auxiliary transistor (M18) will be turn off. On the other hand, if the output voltage of Com_n is "L", the M19 will be also turn off. Therefore, the SR enhancing circuit doesn't increase power consumption in the stable state.

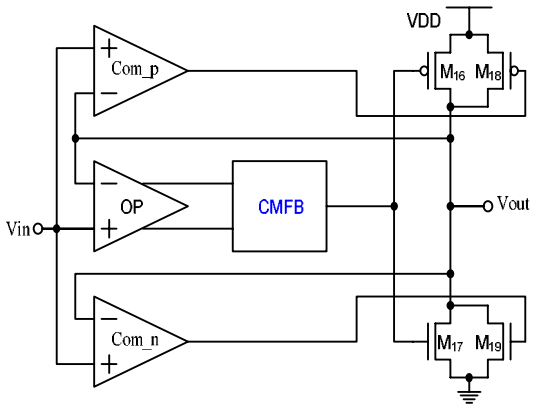

Fig. 1 Block diagram of the high slew rate and low offset voltage buffer for TFT-LCD source driver.

The whole circuit of the proposed buffer is shown in figure 2. The fully-differential input pair was realized with two PMOS (M5, M6) to minimize the noise effect of the input signal. M9-M10 and M11-M12 are two sets of comparators which quickly sense the change of the input transient voltage. M9-M10 is used to sense the input voltage rising edge, and then auxiliary driving transistor, M19, turns on to reduce the rising time. M11-M12 works at falling edge, and then M18 helps discharging and reducing the falling time.

Figure 3 shows the CMFB stage and its small-signal equivalent circuit. M14 and M15 are differential-like input pair and M13 supplies a stable current. The currents of M14 and M15 are controlled by the output voltages of the fully-differential input stage. This provides a negative feedback loop, so Vin and Vout of the buffer in the fig. 2 would become the same voltage level. Therefore, the CMFB stage can provide a common-mode voltage to output stage. The fully-differential output voltages are expressed as follows.

$$V_4 = -\tfrac{1}{2} g_m R_D v_d - \frac{R_D}{\frac{1}{g_m} + 2R} v_c \;;$$

$$V_5 = +\tfrac{1}{2} g_m R_D v_d - \frac{R_D}{\frac{1}{g_m} + 2R} v_c$$

The CMFB output voltage is expressed as follows.

$$V'_o = -(g_{m14} v_4 + g_{m15} v_5)(r_{o14} \| r_{o15} \| r_{013})$$

$$= g'_m \frac{2R_D}{\frac{1}{g_m} + 2R} v_c \cdot (r_{o14} \| r_{o15} \| r_{013})$$

$$g'_m = g_{m14} = g_{m15}$$

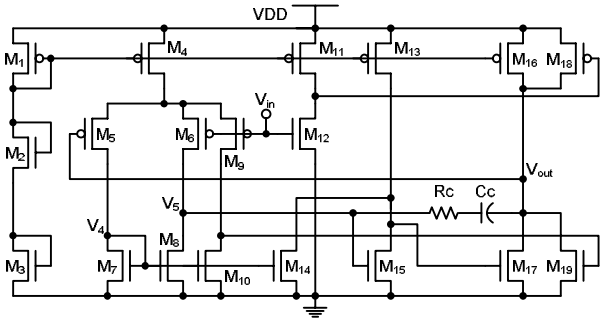

Fig. 2 The proposed buffer for TFT-LCD source driver

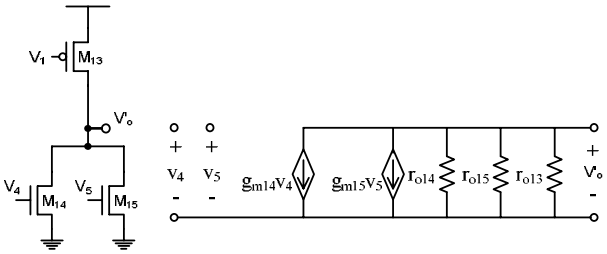

Fig. 3 The CMFB stage and its small-signal equivalent circuit

In this way, by adding the slew rate enhancing circuit and the CMFB stage, the rising/falling time and the systematic offset voltage of the buffer could be reduced. Moreover, the circuit layout was carried out by considering symmetrical architecture and suitable configuration in the fully-differential input stage and the CMFB stage. Thus, the random offset voltage could be minimized.

3. Results

The proposed high slew rate and low offset voltage buffer for TFT-LCD source driver was simulated by using TSMC 0.35-μm CMOS technology. Figure 4 shows the output buffer with a 5-stage R-C network to replace the loads of data lines and pixels in array circuits. Each resistor and capacitor is 2 KΩ and 30 pF, respectively. The power supply VDD is 5 V.

Figure 5 shows the simulated results of the buffer with the input signal of a 100 KHz square wave. In the lower trace, the rising/falling settling time and rising/falling SR are 2.31/0.8 μs and 79.87/625.98 V/μs, respectively.

Figure 6(a) shows the input (solid line) and output (dash line) waveforms and figure 6(b) exhibits the differences between Vin and Vout of the buffer. It is found that the output swing is from 0.0 to 4.6 V. The output voltage range is divided into three regions: 0.0-to-1.2 V, 1.2-to-3.4 V, and 3.4-to-4.6 V, which are corresponding to black, gray, and white gray-level and their maximum offset voltages are 10.36 mV, 1.88 mV, and 6.53 mV, respectively.

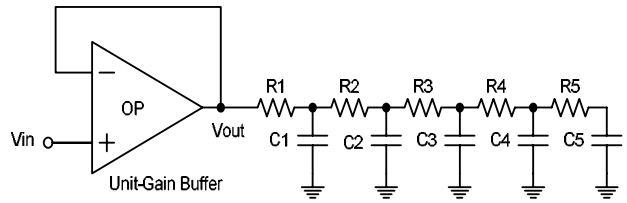

Fig. 4 The buffer with a 5-stage RC load

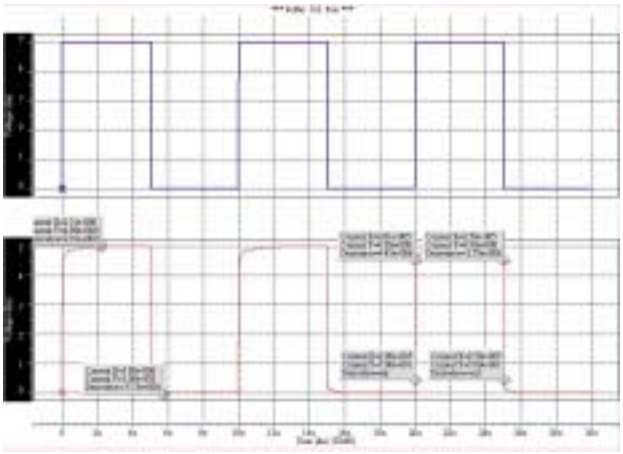

Fig. 5 The simulation results of the proposed buffer with the input signal of a 100 KHz square wave. The lower trace is output waveform.

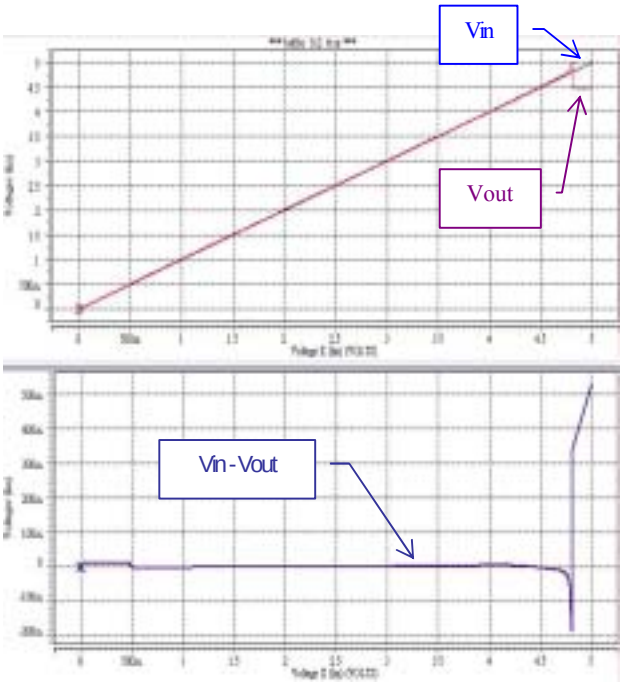

Fig. 6 The simulated results of DC analysis.

Figure 7 shows the results of AC analysis of the buffer. The gain, the phase margin (PM), and the unit-gain bandwidth are 46.4 dB, 54° and 665 MHz, respectively. Therefore, the proposed circuit is suitable for TFT-LCD source driver application with high resolution and high color depth, because of its low offset voltage and high driving capability.

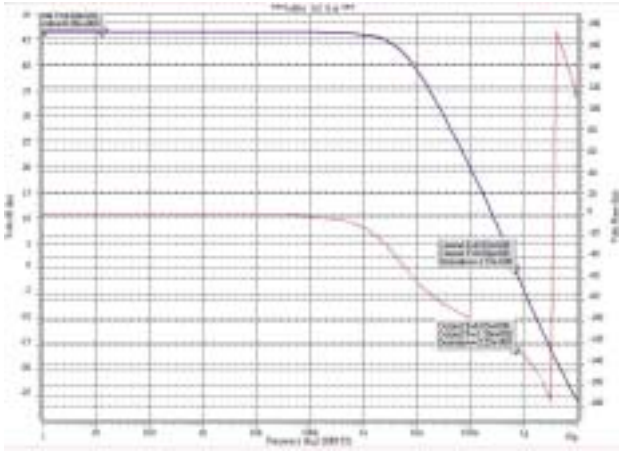

Fig. 7 The simulation results of AC analysis

4. Discussion

The overall simulated performance of the buffer is summarized in table 1. Compared to references [2-3], the proposed buffer could achieve a large output swing without any independent current sources in the buffer. In addition, the proposed buffer reaches faster slew rates and shorter settling times among the single amplifier. In this table, it is also found that low offset voltages below 1.88 mV at mid-gray levels and the power consumption 1.98 mW were achieved.

Table 1 The performance of the buffer in this work

Parameter		Proposed Buffer
Technology		TSMC 0.35μm CMOS
Power Supply		5V
Unit-Gain Bandwidth		665MHz
DC Gain		46.4dB
Phase Margin		54°
Output Swing		0.0-4.6V
Offset voltage (max.)	0.0~1.2V	10.36mV
	1.2~3.4V	1.88mV
	3.4~4.6V	6.53mV
Slew Rate	Rising	79.87V/μs
	Falling	625.98V/μs
Rising Settling Time		2.31μs
Falling Settling Time		0.80μs
Power Consumption		1.98mW
Loading		5-level 2KΩ||30pF network

The fabrication of the proposed buffer is on progress by using a 0.35 μm 2P4M process.

5. Conclusion

The presented high slew rate and low offset voltage buffer for TFT-LCD source driver has been developed and simulated by using a TSMC 0.35-μm CMOS process. By adding two comparators, which sense the rising and falling edges of the input signal, the auxiliary transistors turn on/off to help discharging/charging the output load. By using CMFB circuit, the offset voltage of the buffer can be effectively reduced and controlled within 1.88 mV in the middle gray levels. Therefore, the proposed high slew rate and low offset voltage buffer has a potential to be applied in the source driver for LCD-TVs and large-size TFT-LCD monitors with high color depth and high resolution.

6. Acknowledgements

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7. References

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